

PATENT APPLICATION

In re application of: Ji-Young Kim and Hyoung-Sub Kim
Serial No. Not yet assigned Examiner: Not yet assigned
Filed: August 25, 2003 Group Art Unit: Not yet Assigned
For: INTEGRATION METHOD OF A SEMICONDUCTOR DEVICE HAVING A RECESSED GATE ELECTRODE

**INFORMATION DISCLOSURE CITATION
FORM PTO-1449 (Modified)**

U.S. PATENT DOCUMENTS

<u>Exam</u>	<u>Init</u>	<u>Ref</u>	<u>Document Number</u>	<u>Issue Date</u>	<u>Name</u>	<u>Class</u>	<u>Sub Class</u>
_____	_____	_____	6,063,669	5/16/2000	Takaishi	_____	_____

FOREIGN PATENT DOCUMENTS

<u>Exam</u>	<u>Init</u>	<u>Ref</u>	<u>Document Number</u>	<u>Publication Date</u>	<u>Country</u>	<u>Name</u>
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OTHER DOCUMENTS

<u>Exam</u>	<u>Init</u>	<u>Ref</u>	<u>Author, Title, Date, Pertinent Pages, Etc.)</u>
_____	_____	_____	_____

Examiner: _____

Date Considered: _____